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EXAMINER	
SINGH, DALIP K	
ART UNIT	**PAPER NUMBER**
2628	

DATE MAILED: 04/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,215	FOULADI ET AL.	
	Examiner	Art Unit	
	Dalip K. Singh	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29,31-43,55-76 and 81-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35,57,58 and 82-84* is/are allowed.

6)☒ Claim(s) *1-29,31-34,36-43,55,56,59-76 and 81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/16/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's Request for Continued Examination (RCE) dated November 16, 2005, in response to PTO Office Action dated November 10, 2005. The addition of claim(s) 82-83 have been noted and entered in the record, and applicant's remarks have been carefully considered resulting in the action as set forth herein below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim(s) 1-4, 7, 9, 10, 11-18, 31-32, 36-38, 55, 56, 60-62, 65-76, 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,112,267 to McCormack et al. in view of U.S. Patent No. 5,838,334 to Dye, and further in view of US 6,553,426 to Hölzle et al.

a. Regarding claim 1, McCormack et al. **discloses**: a producer (processor 300, Figure 1a) that outputs graphics commands, a consumer (graphics processor 700, Figure 1a) that consumes the graphics commands outputted by the producer (processor 300, Figure 1), and a ***shared*** memory (main memory 200, cache memory 310, off-chip cache 400;*...a processor-memory bus 610 in communication with the main memory 200 and the processor 300; an I/O bus 630 in communication with the I/O device 700...col; 6, lines 25-30;...referring to Fig. 1a, the processor 300 generates data to be eventually read by the graphics device 700..the controller 500 and the graphics device 700 cooperate to DMA read data from various locations in the memory hierarchy 200, 310, and 400 ...col.], lines 60-67; col. 8, lines 1-11*) coupled between the producer (processor

300, Figure 1) and the consumer (graphics processor 700, Figure 1), the ***shared*** memory (main memory 200, cache memory 310, off-chip cache 400) storing at least one buffer (third ring buffer 212) receives and temporarily stores graphics commands outputted by the producer (processor 300, Figure 1a) for delivery to the consumer (graphics processor 700, Figure 1) (...the processor 300 generates data to be...read by the graphics device 700...col. 7, lines 60-67), wherein the producer (processor 300, Figure 1a) and the consumer (graphics processor 700, Figure 1) are capable of accessing said buffer (third ring buffer 212) independently of one another (...the processor 300 can write data to buffers 312, 412 or 212...the graphics device 700 can read data from buffers 312, 412 or 212...the dynamic and independent functioning of steps 900 and steps 800 permits...the...writes...and reads...col. 8, lines 5-25). However, McCormack et al. **fails to disclose** wherein said buffers store inline commands calling display lists stored elsewhere in said ***shared*** memory. Dye **discloses** a display list operation which details pointer manipulations for display list memory buffers (...the windows ID list and the windows workspace buffer comprise memory areas in the system memory 110 used...the display memory section or buffer includes a plurality of memory areas...and pointers assembled I the display refresh list are used to reference this data...or only the pointers in the display refresh list are manipulated...the term "display memory" as used...is not intended to connote a single frame buffer memory...but rather stores video data for windows or objects in a plurality of respective memory areas...col. 11, lines 30-67; col. 22, lines 15-67; col. 23; lines 1-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by McCormack et al. with the "display list memory buffers utilizing pointer references" as taught by Dye **because** it requires no data movement thus reducing system bandwidth requirements resulting in improved system performance. However, McCormack-Dye

combination **fails to address** wherein inline commands calling display lists comprise further graphics commands for execution by said graphics hardware. The specification of the instant application describes this at page 25, lines 1-13 (...whereby an entry in a FIFO buffer 210 can call a display list-almost as if it were a function call...the graphics processor 114 temporarily ceases reading graphics commands from FIFO buffer 210 and instead begins reading commands from a display list 212 stored elsewhere in main memory 112...). Hölzle et al. **discloses** a function that is external to the routine, and the function, once called, begins executing. Eventually, the function returns to the routine with the function returning to a location in routine that is identified by a normal return address (col. 3, lines 60-67; col. 4, lines 1-5). Hölzle et al. **further discloses** wherein many programs, which include routines, are written such that a program calls "external" functions which may not be included within the program and the functions that are called must eventually return into the routine (col. 1, lines 40-56, Fig. 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify McCormack-Dye combination with the feature "function call where external functions are called in which are not within the program; are executed and then execution returns back into the routine" as taught by Hölzle et al. **because** this allows computer resources to be used more efficiently.

b. Regarding claim 2, McCormack et al. **discloses** wherein the producer (processor 300) and the consumer (graphics processor 700) have independent read and/or write pointers (head pointers 726 & 736, tail pointers 728 & 736, Fig. 3a).

c. Regarding claims 3-4, McCormack et al. **discloses** wherein the ***shared*** memory (main memory 200, cache memory 310, off-chip cache 400;...*a processor-memory bus 610 in communication with the main memory 200 and the processor 300; an I/O bus 630 in communication with the I/O device 700...col; 6, lines 25-30;...referring to Fig.*

1a, the processor 300 generates data to be eventually read by the graphics device 700..the controller 500 and the graphics device 700 cooperate to DMA read data from various locations in the memory hierarchy 200, 310, and 400 ...col. 7, lines 60-67; col. 8, lines 1-11) stores plural variable sized buffers (a first ring buffer 312, second ring buffer 412, third ring buffer 212) disposed at selected locations within the main memory (...a first ring buffer 312...fit in the on-chip cache 310...a second ring buffer 412...a third ring buffer 212...col. 6, lines 10-31) each of which can be independently accessed by the producer (processor 300) and/or the consumer (graphics processor 700) (...the processor 300 can write data to buffers 312, 412 or 212...the graphics device 700 can read data from buffers 312, 412 or 212...the dynamic and independent functioning of steps 900 and steps 800 permits...the...writes...and reads...col. 8, lines 5-25).

d. Regarding claim 7, it is similar in scope to claim 2 and is rejected under the same rationale.

e. Regarding claim 9, McCormack et al. as modified by Dye **discloses** consumer (graphics processor 700, Figure 1) (...the processor 300 generates data to be...read by the graphics device 700...col. 7, lines 60-67) to consume the display list (...the buffer 312 fills data written by the processor 300...the graphics device 700 must read all of the data from the buffer 312 before reading any data from the buffer 412...col. 12, lines 1-20) the producer stores elsewhere within the ***shared*** memory (main memory 200, cache memory 310, off-chip cache 400;*...a processor-memory bus 610 in communication with the main memory 200 and the processor 300; an I/O bus 630 in communication with the I/O device 700...col; 6, lines 25-30;...referring to Fig. 1a, the processor 300 generates data to be eventually read by the graphics device 700..the controller 500 and the graphics device 700 cooperate to DMA read data from various locations in the memory hierarchy 200, 310, and 400 ...col. 7, lines 60-67; col. 8, lines 1-11 as per*

McCormack;...before reading any data from the buffer 412...col. 12, lines 15-20 as per Dye), and to resume consuming graphics commands from the first buffer after consuming the graphics commands stored elsewhere (Dye **discloses** a display list operation which details pointer manipulations for display list memory b fers (...the windows ID list and the windows workspace buffer comprise memory areas in the system memory 110 used...the display memory section or buffer includes a plurality of memory areas...and pointers assembled I the display refresh list are used to reference this data...or only the pointers in the display refresh list are manipulated...the term "display memory" as used...is not intended to connote a single frame buffer memory...but rather stores video data for windows or objects in a plurality of respective memory areas...col. 11, lines 30-67; col. 22, lines 15-67; col. 23; lines 1-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by McCormack et al. with the "display list memory buffers utilizing pointer references" as taught by Dye **because** it requires no data movement thus reducing system bandwidth requirements resulting in improved system performance.

f. Regarding claims 10 and 66, McCormack et al. **discloses** read command specifying a starting address (...the graphics device ...commences reading data from the buffer...starting at the address given by the head pointer 736...col. 12, lines 35-37) and **implicitly discloses** a length of a display list.

g. Regarding claims 11 and 12, McCormack et al. **discloses** the buffer providing circular first-in-first-out access (...the plurality of buffers can be configured as ring buffers...col. 5, lines 35-40).

h. Regarding claims 13 and 69, McCormack et al. **implicitly** discloses wherein the buffer can be selectively attached to both the producer and the consumer simultaneously

(...the use of multiple buffers and the dynamic switching between buffers enhances the flow of data from the processor, via the buffers, to the I/O device...col. 5, lines 3-6).

i. Regarding claims 14-18, McCormack et al. **discloses** use of multiple buffers and the dynamic switching between buffers which enhances the flow of data from the processor, via the buffers, to the I/O device (col. 5, lines 3-6).

j. Regarding claim 31, McCormack et al. **discloses** wherein the producer comprises a processor (processor 300, Figure 1a) and the consumer comprises a graphics processor (graphics processor 700, Figure 1a) including a graphics pipeline. the storage device comprises the ***shared*** memory (main memory 200, cache memory 310, off-chip cache 400;*...a processor-memory bus 610 in communication with the main memory 200 and the processor 300; an I/O bus 630 in communication with the I/O device 700...col; 6, lines 25-30;...referring to Fig. 1a, the processor 300 generates data to be eventually read by the graphics device 700..the controller 500 and the graphics device 700 cooperate to DMA read data from various locations in the memory hierarchy 200, 310, and 400 ...col. 7, lines 60-67; col. 8, lines 1-11*), and the producer dynamically allocates said buffer within the main system memory (...the use of multiple buffers and the dynamic switching between buffers enhances the flow of data from the processor, via the buffers, to the I/O device...col. 5, lines 3-6).

a. Regarding claim 32, it is similar in scope to claim 2 above and is rejected under the same rationale.

k. Regarding claim 36, it is similar in scope to claim 2 above and is rejected under the same rationale.

l. Regarding claim 37, it is similar in scope to claim 1 above and is rejected under the same rationale.

m. Regarding claim 38, it is similar in scope to claim 2 above and is rejected under the same rationale.

n. Regarding claim 55, it is similar in scope to claim 1 above and is rejected under the same rationale.

o. Regarding claim 56, official notice is taken that both the concept and advantage of circular buffer in general is well known and expected in the graphics/data processing art.

p. Regarding claim 60, it is similar in scope to claim 4 above and is rejected under the same rationale.

q. Regarding claim 61, it is similar in scope to claim 5 above and is rejected under the same rationale.

r. Regarding claim 62, it is similar in scope to claim 2 above and is rejected under the same rationale.

s. Regarding claim 65, it is similar in scope to claim 9 above and is rejected under the same rationale.

t. Regarding claim 67, it is similar in scope to claim 11 above and is rejected under the same rationale.

u. Regarding claim 68, it is similar in scope to claim 12 above and is rejected under the same rationale.

v. Regarding claim 70, it is similar in scope to claim 14 above and is rejected under the same rationale.

w. Regarding claim 71, it is similar in scope to claim 15 above and is rejected under the same rationale.

x. Regarding claim 72, it is similar in scope to claim 16 above and is rejected under the same rationale.

y. Regarding claim 73, it is similar in scope to claim 17 above and is rejected under the same rationale.

z. Regarding claim 74, it is similar in scope to claim 18 above and is rejected under the same rationale.

aa. Regarding claim 75, it is similar in scope to claim 32 above and is rejected under the same rationale.

bb. Regarding claim 76, it is similar in scope to claim 55 above and is rejected under the same rationale.

cc. Regarding claim 81, it is similar in scope to claim 76 above and is rejected under the same rationale.

2. Claims 5, 6, 8, 33, 34, 39-41, 59, 63 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,112,267 to McCormack et al. in view of U.S. Patent No. 5,838,334 to Dye., and further in view of US 6,553,426 to Hölzle et al. as applied to claim 1 above, and further in view of U.S. Patent No. 6,470,403 B1 to Houg.

a. Regarding claim 5, McCormack-Dye-Hölzle combination **discloses** plural buffers in the form of ring buffers. McCormack et al. **teaches** data writes by the processor and data reads by the graphics device to be simultaneously directed at different buffers located at different levels in the memory hierarchy (col. 4, lines 60-67). These plurality of buffers are preferentially selected as write buffers to store data transmitted by the processor (col. 5, lines 19-23).The graphics device 700 (consumer) always reads data from the presently active buffer. Fig. 3a shows locations in ring buffer locations containing data awaiting a read by the graphics device 700 (consumer); and

other locations available for data writes by the processor 300 (producer). Processor 300 (producer) and the graphics device 700 (consumer) utilize head pointers and tail pointers similar to the write pointer for determining quantity of data in a buffer (col. 7, lines 45-60). Further, data reads by the graphics device 700 and data writes by the processor 300 as shown in Fig. 5 and Fig. 6 function separately (col. 8, lines 26-36) which implies that some plurality of buffers are reserved for writes by the producer only and some for reads only by the consumer. However, McCormack-Dye-Hölzle combination **is silent about** maintaining an independent read and write pointers. Houg **discloses** independent read and write pointers (col. 3, lines 6-20). Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify McCormack-Dye-Hölzle combination "read buffers that are separated from the write buffers" with the feature "independent read and write pointers" as taught by Houg **because** it is an efficient way of preventing overflow or underflow of buffers (col. 2, lines 65-67).

b. Regarding claim 6, McCormack-Dye-Hölzle combination as modified by Houg **discloses** wherein the consumer (graphics processor 12, Figure 1) selectively increments the consumer write pointer (112a, Houg:col. 3, lines 6-20) in response to the producer (host processor 10, Figure 1) writing to the active buffer the **motivation** for doing being preventing overflow or underflow of buffers (Houg: col. 2, lines 65-67).

c. Regarding claim 8, wherein the consumer increments the consumer read pointer, and suspends reading from the active buffer when the incremented consumer read pointer has a predetermined relationship with the consumer write pointer, the specification discloses on pages 22-24 that once the write pointer encounters the read pointer, it ceases writing to avoid overwriting valid data or in other words buffer has been read completely. McCormack-Dye-Hölzle combination as modified by Houg

discloses read pointer incrementing as the consumer reads, and suspending reading from the buffer based on a predetermined relationship with the consumer write pointer (...as information is read from the...buffer...the read pointer...advances until it may catch up with the write pointer...at which time...buffer...is empty...col. 3, lines 18-20). Therefore, it would have been obvious to a person of ordinary skill in the art at the time was made to modify McCormack-Dye-Hölzle combination with the feature "read pointer reading, suspending reading based on a predetermined relationship with write pointer" as taught by Houg **because** FIFO buffer has been emptied and thus prevents underflow condition (col. 3, lines 65-67).

d. Regarding claim 33, it is similar in scope to claim 8 above and is rejected under the same rationale.

e. Regarding claim 34, it is similar in scope to claim 6 above and is rejected under the same rationale.

f. Regarding claim 39, it is similar in scope to claim 8 above and is rejected under the same rationale.

g. Regarding claim 40, it is similar in scope to claim 8 above and is rejected under the same rationale.

h. Regarding claim 41, it is similar in scope to claim 5 above and is rejected under the same rationale.

i. Regarding claim 59, it is similar in scope to claim 5 above and is rejected under the same rationale.

j. Regarding claim 63, it is similar in scope to claim 8 above and is rejected under the same rationale.

k. Regarding claim 64, it is similar in scope to claim 6 above and is rejected under the same rationale.

3. Claims 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,112,267 to McCormack et al. in view of U.S. Patent No. 5,838,334 to Dye. and further in view of US 6,553,426 to Hölzle et al. as applied to claim 1 above, and further in view of U.S. Patent No. 6,674,805 B1 to Kovacevic.

a. Regarding claims 19-23, McCormack-Dye-Hölzle combination is **silent** about buffer having a maximum size, the producer setting the size of the buffer, dynamically sizing up the buffer to store a frame of graphics commands, producer declaring the buffer by issuing a graphics buffer initialization command specifying buffer starting address and buffer length, buffer length being a multiple of 32 bytes and having a minimum size of 64 KB, and wherein the producer may write a breakpoint into the buffer that suspends graphics commands upon encountering the breakpoint. Kovacevic et al. **discloses** use of system circular buffers wherein the host processor (producer) specifies buffer start address and length of the buffer (col. 20, lines 15-23). Kovacevic et al. **teachings** are therefore taken in the context of ring buffer management in a graphics system and therefore cover the limitations wherein buffer maximum size, sizing up the ring buffer to accommodate a frame of graphics commands, buffer starting address and buffer length, and **implicitly** also cover buffer length of a certain multiple of bytes with minimum size. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify McCormack-Dye with the feature "physical memory location and size of the ring buffer" as taught by Kovacevic et al. **because** it provides for efficient ring buffer management.

4. Claim(s) 24 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,112,267 to McCormack et al. in view of U.S. Patent No. 5,838,334 to Dye. and

further in view of US 6,553,426 to Hölzle et al. as applied to claim 1 above, and further in view of U.S. Patent No. 6,674,805 B1 to Kovacevic and further in view of U.S. Patent No. 5,754,839 to Pardo et al.

a. Regarding claims 24 and 42, McCormack-Dye- Hölzle-Kovacevic combination **is silent** about producer writing a breakpoint into the buffer resulting in suspension of graphics commands being consumed by consumer. Pardo et al. **discloses** storing breakpoint information in history buffer. Pardo et al. **is dealing** with implementation of watchpoints and breakpoints in a data processing system, and it can be argued that it is not relevant to the instant claim limitation, but Pardo et al. **does disclose** writing of a breakpoint into a buffer and is therefore pertinent to the instant claim. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify McCormack-Dye- Hölzle-Kovacevic combination with the feature "breakpoint written into a buffer resulting "in suspension of commands"" as taught by Pardo et al. **because** it results in efficient program handling of processing system (col. 8, lines 53-56).

5. Claims 25-29 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,112,267 to McCormack et al. in view of U.S. Patent No. 5,838,334 to Dye. and further in view of US 6,553,426 to Hölzle et al. as applied to claim 1 above, and further in view of U.S. Patent No. 6,038,619 to Berning et al.

a. Regarding claims 25-29, McCormack-Dye-Hölzle **is silent** in describing the details of buffer management as far as overflow status indicator, status registers, pointer positions, buffer overflow, flow control logic to prevent writes from overrunning reads; wrapping read and write pointers from a last location to a first location. Berning et al. **discloses** management of a circular buffer while overflowing and underflowing, pointer increments, direction of closure between pointers, taking care reading pointer is not

overtaking the writing pointer (col. 5, lines 54-67; col. 6, lines 1-8). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify McCormack-Dye-Hölzle with the feature "circular buffer overflow and underflow management" as taught by Berning et al. **because** it results in efficient circular buffer performance.

b. Regarding claim 43, it is similar in scope to claim 25 above and is rejected under the same rationale.

Allowable Subject Matter

6. Claim(s) 35, 57, 58, 82, 83, and 84 are allowed. Prior art fails to disclose read/write pointers associated with a producer and a consumer involving graphics commands wherein the consumer maintains a write pointer independent of the producer write pointer, and a consumer read pointer that is independent of the producer read pointer; and wherein a configuration command specifies auto-incrementation of the consumer write pointer in response to producer writing to the buffer; producer writing command referencing a second set of graphics elsewhere within a storage device and consumer consuming first set of graphics commands while encountering the referencing command consumes the second set of commands referenced as per independent claims 35, 57 and 58. Also, prior art fails to disclose wherein in response to encountering the calling command, reading the stored display commands in the display list and responsively generating at least a further portion of said first image in said frame buffer memory; writing additional commands into the same or different memory buffer, said additional commands including at least a second set of graphics commands and at least one calling command that calls the same further, prestored list of display commands; at least some the second stet of graphics commands to generate at least a portion of a second image in the same or different frame buffer memory; and reusing said further, stored list of display commands to generate said second image as per independent claim 82.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**. The examiner can normally be reached on Mon-Friday (10:00AM-6: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Ulka Chauhan**, can be reached at **(571) 272-7782**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Please note that the new Central Official FAX number for application specific communications with the USPTO is **571-273-8300** (effective July 15, 2005).

Dalip K. Singh
Examiner, Art Unit 2628
dks
April 5, 2006